U.S. Department of Commerce, Patent and Trademark Office	Atty. Docket No.	Serial No.
	M-15327 US	10/772,932
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Chia-Shun Hsiao et al.	
	Filing Date	Group
	Feb. 4, 2004	2818

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
CAL	AA	6,403,417	06-2002	Chien et al.			
CAL	AB	6,451,708	09-2002	Ha			
	AC						
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

CAL	AL	Naruke, K.; Yamada, S.; Obi, E.; Taguchi, S.; and Wada, M. "A New Flash-Erase EEPROM Cell with A Sidewall Select-Gate On Its Source Side," 1989 IEEE, pp. 604-606.
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CAL	AP	Mih, Rebecca et al. "0.18um Modular Triple Self-Aligned Embedded Split-Gate Flash Memory," 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 120-121.
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Examiner CAL	Date Considered 7/25/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office	Atty. Docket No.	Serial No.
	M-15327 US	Unassigned
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
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	Filing Date	Group
	Herewith	Unassigned

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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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CH	AB	6,355,524	12 Mar. 2002	Tuan et al.			
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Foreign Patent Documents

		Document	Date	Country	Class	Subclass	Translation Yes	Translation No
	AL							
	AM							
	AN							
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

CH	AQ	K. Naruke et al., "A New Flash-Erase EEPROM Cell with a Sidewall Select-Gate on Its Source Side", IEDM Technical Digest 1989, pages 603-606.
CH	AR	United States Application No.: 10/402,698 filed March 28, 2003 by Chung et al.
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Examiner	Date Considered 7/25/05

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